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LSI Logic Corporation  
Legal Department – IP  
1621 Barber Lane, MS D-106  
Milpitas, CA 95035

Date February 24, 2006

Number of pages including cover sheet 2

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Mail Stop Status Request  
TC 2825  
Fax No. 571-273-8300  
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From: Connie del Castillo  
Intellectual Property Paralegal  
Telephone No. (408) 433-7191  
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**REMARKS:**

Urgent  For your review  Reply ASAP  Please comment

Application Number: 10/697,357  
Filing date: October 29, 2003  
First named inventor: Viswanathan Lakshmanan et al.  
Attorney docket number: 03-1772 / 81610

Transmitted herewith for filing via facsimile:

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PAGE 1/2 \* RCVD AT 2/24/2006 10:44:26 PM [Eastern Standard Time] \* SVR:USPTO-EFXRF-68 \* DNIS:2738300 \* CSID:4084337460 \* DURATION (mm:ss):00:58

FEB 24 2006

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

<u>In re Application of :</u>	§		
Viswanathan Lakshmanan et. al.			
<u>Serial No. :</u>	10/697,357	<u>Group Art Unit :</u>	2825
<u>Filed :</u>	October 29, 2003	<u>Examiner :</u>	
<u>For :</u>	Method Of Partitioning An Integrated Circuit Design For Physical Design Verification	<u>Atty Docket :</u>	81610 / 03-1772
		§	
		§	
		§	
		§	
		§	
		§	

STATUS REQUEST

Commissioner for Patents  
P. O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Applicants request a status of the above referenced application. Please mail the status notification to the address stated below.

Respectfully submitted,



Timothy Croll, Ph: [+1] 408-433-7191

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